# THE UNITED STATES PATENT AND TRADEMARK OFFICE Attorney Docket No. 13309US04

1774 Application of:	) <u>CERTIFICATE OF MAILING</u>	<u>J</u>
MORTEZA CYRUS AFGHAHI	) I hereby certify that this corresponde	
Serial No. 10/736,350	<ul> <li>is being deposited with the United St</li> <li>Postal Service as first class mail in a envelope addressed to: Commission</li> </ul>	n
Filed: December 15, 2003	) Patents, P.O. Box 1450, Alexandria, 22313-1450 on March 3, 2004.	
For: DENSE CONTENT	)	
ADDRESSABLE MEMORY CELL	) 1 1 1 1	
Examiner: to be assigned	) By: Konald E. Larson ) Reg. No. 24,478	<b>~</b>
Group Art Unit: to be assigned	) Attorney for Applicant	

# TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT AFTER APPLICATION FILING DATE

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

## **ENCLOSURES**

Enclosed are the following:

- \* A completed PTO form 1449 (modified) which has 1 one page.
- \* No copies of the seven (7) listed references on the 1449 are enclosed since they were previously provided in the parent case, Serial No. 10/127,175.
- \* A copy of a Partial European Search Report for the European International Application, No. 03009170.6 corresponding to the parent of the above application.

### FEE DETERMINATION

\* No fee is believed to be due because:

The applicant believes that this statement and enclosures are being filed before the

first Office Action on the merits has been mailed by the PTO. The basis of this belief is that no Office Action on the merits appears to have been received by the undersigned to date.

#### FEE PAYMENT

The following arrangements have been made to pay the fees calculated above:

\* No fee is believed to be due.

The Commissioner is hereby authorized to charge any additional fees which are presently required, or credit any overpayment, to Deposit Account No. 13-0017.

# REQUEST FOR CONSIDERATION

This paper and enclosures are believed to be entitled to consideration under 37 C.F.R. § 1.97, based on the facts stated above. The Examiner is requested to initial both copies of the enclosed PTO-1449 (modified) and return one copy to the applicants to indicate consideration of the enclosed references.

This submission is in no way intended as an admission that the cited references constitute prior art under any subsection of 35 U.S.C. § 102. Applicant expressly retains the right to take any actions necessary to remove the cited references from the available prior art.

Respectfully submitted,

Dated: March 23, 2004

Ronald E. Larson Reg. No. 24,478

Attorney for Applicant

McAndrews, Held & Malloy, Ltd. 500 West Madison Street, 34th Floor Chicago, IL 60661 (312) 775-8000

FORM PTO-1449	SERIAL NO.	CASE NO.
TRADER	10/736,350	13309US04
LIST OF PATENTS AND PUBLICATIONS FOR	FILING DATE	GROUP ART UNIT
APPLICANT'S INFORMATION DISCLOSURE	December 15, 2003	to be assigned
STATEMENT		_
(use several sheets if necessary)	APPLICANT(S): Mortieza Cyrus Afghahi	

REFERENCE DESIGNATION	U.S. PATENT DOCUMENTS
ILLI FILLIOF DEGICIANTICIA	U.U. I AI EIAI DUUUNEIA

EXAMINER	DOCUMENT			CLASS/	FILING
INITIAL	NUMBER	DATE	NAME	SUBCLASS	DATE
	3,609,710	09/28/1971	Browne	340/173	05/29/1969
	5,475,633	12/12/1995	Mehalel	365/154	06/01/1994

### FOREIGN PATENT DOCUMENTS

, o						
EXAMINER	DOCUMENT			CLASS/	TRANS	LATION
INITIAL	NUMBER	DATE	COUNTRY	SUBCLASS	YES	МО

EXAMINER INITIAL	OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
	Miyatake, H. et al., "A Design For High-Speed Low-Power CMOS Fully Parallel Content-Addressable Memory Macros", <i>IEEE Journal of Solid-State Circuits</i> , IEEE Inc., Vol. 36, No. 6, June 2001, pages 956-968
	Noda, K. et al., "A 1.9-µm² Loadless CMOS Four-Transistor SRAM Cell in a 0.18-µm Logic Technology", Electron Devices Meeting, 1998. <i>IEDM '98 Technical Digest.</i> , International San Francisco, CA, 1998, pages 643-646
	Grosspietsch, K.E., "Associative Processors and Memories: A Survey", <i>IEEE Micro</i> , Vol. 12, No. 3, June 1, 1992, pages 12-19
	"High Performance Static Content Addressable Memory Cell", IBM Technical Disclosure Bulletin, IBM Corp., Vol. 32, No. 3A, August 1, 1989 page 478
	Fitchen, Franklin C., "Transistor Circuit Analysis And Design", D. Van Nostrand Co. (1960), pages 304-314

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.